DMOS DUAL ½-H-BRIDGE MOTOR DRIVERS

Check for Samples: DRV8816

FEATURES

- **Low ON-Resistance (0.83-Ω) Outputs**
- **Individual ½-H bridge control**
- **Low-Power Sleep Mode**
- **100% PWM Supported**
- **8.0 - 38 V Operating Supply Voltage Range**
- **Thermally Enhanced Surface Mount Package**
- **Configurable Overcurrent Limit**
- **Protection Features**
  - **VBB Undervoltage Lockout (UVLO)**
  - **Charge Pump Undervoltage (CPUV)**
  - **Overcurrent Protection (OCP)**
  - **Short-to-Supply Protection (STS)**
  - **Short-to-Ground Protection (STG)**
  - **Overtemperature Warning (OTW)**
  - **Overtemperature Shutdown (OTS)**
  - **Fault Condition Indication Pin (nFAULT)**

APPLICATIONS

- **Printers**
- **Industrial Automation**

DESCRIPTION

The DRV8816 provides a versatile power driver solution with two independent ½-H bridge drivers. The device can drive one brushed DC motor or one winding of a stepper motor, as well as other devices like solenoids. A simple INx/ENx interface allows easy interfacing to controller circuits.

The output stages use N-channel power MOSFET's configured as ½-H-bridges. The DRV8816 is capable of peak output currents up to ±2.8 A and operating voltages up to 38 V. An internal charge pump generates needed gate drive voltages.

A low-power sleep mode is provided which shuts down internal circuitry to achieve very low quiescent current draw. This sleep mode can be set using a dedicated nSLEEP pin.

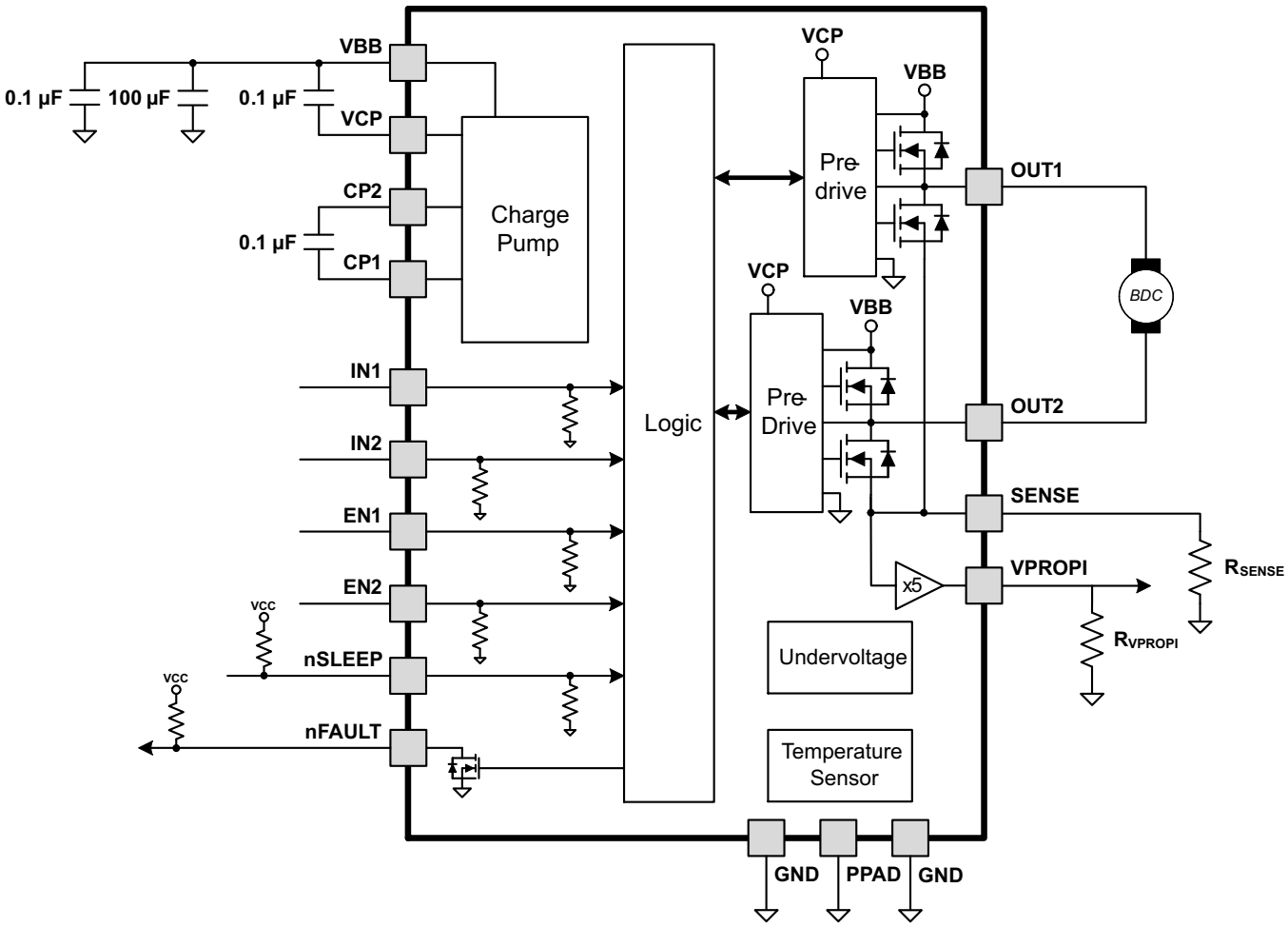
Internal protection functions are provided for under voltage lockout, charge pump fault, overcurrent protection, short-to-supply protection, short-to-ground protection, overtemperature warning, and overtemperature shutdown. Fault conditions are indicated via an nFAULT pin

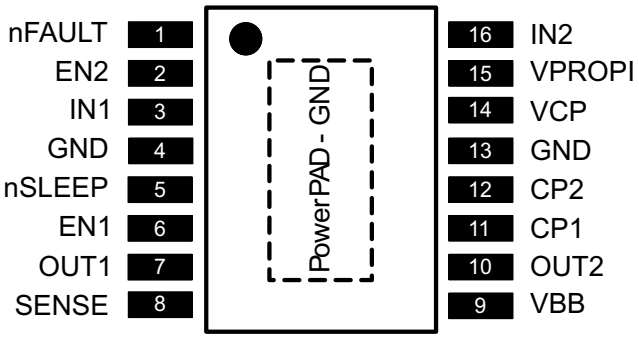
The DRV8816 is packaged in a 16 pin HTSSOP package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BLOCK DIAGRAM





TERMINAL FUNCTIONS

Name	Pin	Type	Description	Comments
Power and Ground				
VBB	9	PWR	Power supply	Connect to motor supply voltage; bypass to GND with a 0.1 µF plus a 100 µF capacitor rated for VBB
GND	4, 13	PWR	Device ground	Must be connected to ground
VCP	14	O	Charge pump output	Connect a 16 V, 0.1 µF ceramic capacitor to VBB
CP1	11	-	Charge pump switching node	Connect a 0.1 µF X7R capacitor rated for VBB between CP1 and CP2
CP2	12	-		
Control				
IN1	3	I	½-H bridge control	Logic high enables the high side ½-H bridge FET; logic low enables the low side FET; internal pulldown
IN2	16			
EN1	6	I	½-H bridge enable	Logic high enables ½-H bridge output; logic low puts the FETs in HI-Z; internal pulldown
EN2	2			
nSLEEP	5	I	Device sleep mode	Pull logic low to put device into a low-power sleep mode; internal pulldown
nFAULT	1	O	Fault indication pin	Pulled logic low with fault condition; open-drain output requires an external pullup
Output				
OUT1	7	O	½-H bridge output	
OUT2	10	O	½-H bridge output	
SENSE	8	O	H-bridge low-side connect	Connect directly to GND or through a sense resistor to set OCP
VPROPI				
VPROPI	15	O	Current-proportional output	

EXTERNAL COMPONENTS

Component	Pin 1	Pin 2	Recommended
C_{VBB1}	VBB	GND	0.1 µF capacitor rated for VBB
C_{VBB1}	VBB	GND	100 µF capacitor rated for VBB
C_{VCP}	VCP	VBB	16 V, 0.1 µF ceramic capacitor
R_{nFAULT}	VCC (1)	nFAULT	> 1 kΩ
R_{SENSE}	SENSE	GND	Optional low-side sense resistor connected to shunt

(1) VCC is not a pin on the DRV8816, but a VCC supply voltage pullup is required for open-drain output nFAULT

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VBB	Load supply voltage	-0.6	40	V
	Charge Pump Voltage (VCP, CP+)	-0.6	VBB + 7	V
	Charge pump negative switching pin range (CP-)	-0.6	VBB	V
VDD	Digital pin voltage range (IN1, IN2, EN1, EN2, nSLEEP, nFAULT)	–0.3	7	V
	VBB to OUTx	-0.6	40	V
	OUTx to SENSE	-0.6	40	V
V_{Sense}	Sense voltage (SENSE)	-0.5	1.0	v
	H-bridge output current (OUT1, OUT2, SENSE)	0	2.8	A
	VPROPI pin voltage range (VPROPI)	-0.3	3.6	V
T_A	Operating ambient temperature	-40	85	°C
T_j	Operating junction temperature	-40	190	
T_{stg}	Storage temperature range	-40	125	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE PROTECTION

	MIN	MAX	UNIT
HBM on any other pin	2000		V
Charge Device Model (CDM)	500		

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8816 PWP - HTSSOP 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	43.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	30.8	
θ_{JB}	Junction-to-board thermal resistance(4)	25.3	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.1	
ψ_{JB}	Junction-to-board characterization parameter(6)	25	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	5.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	MAX	UNIT
VBB	Power supply voltage range	8	38	V
VCC	Logic voltage		5.5	V
f_{PWM}	Applied PWM signal (IN1 and IN2)		100	kHz
I_{OUT}	H-bridge output current		2.8	A
T_A	Ambient temperature	–40	85	°C

(1) Power dissipation and thermal limits must be observed.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLIES (VBB)							
VBB	VBB operating voltage			8		38	V
I_{VBB}	VBB operating supply current	f_{PWM} < 50 kHz			6		mA
		Charge pump on, Outputs disabled			3.2		mA
I_{VBBQ}	VBB sleep-mode supply current	nSLEEP = 0, T_J = 25°C				10	µA
CONTROL INPUTS (IN1, IN2, EN1, EN2, nSLEEP)							
V_{IL}	Input logic low voltage	IN1, IN2, EN1, EN2	V_{IN} = 0.8 V	0		0.8	V
V_{IH}	Input logic high voltage		V_{IN} = 2.0 V	2		5.5	
I_{IL}	Input logic low current	IN1, IN2, EN2	V_{IN} = 0.8 V	–20		+20	µA
I_{IH}	Input logic high current		V_{IN} = 2.0 V			20	
I_{IL}	Input logic low current	EN1	V_{IN} = 0.8 V		16	40	µA
I_{IH}	Input logic high current		V_{IN} = 2.0 V		40	100	
V_{IL}	Input logic low voltage	nSLEEP	V_{IN} = 0.8 V			0.8	V
V_{IH}	Input logic high voltage		V_{IN} = 2.8 V	2.2			V
I_{IL}	Input logic low current		V_{IN} = 0.8 V			10	µA
I_{IH}	Input logic high current		V_{IN} = 2.8 V		27	50	
R_{PD}	Pulldown resistance				100		kΩ
SERIAL AND CONTROL OUTPUT (nFAULT)							
V_{OL}	Output logic low voltage	I_{sink} = 1 mA				0.4	V
DMOS DRIVERS (OUT1, OUT2, SENSE)							
$R_{ds(ON)}$	Output ON resistance	Source driver, I_{OUT} = –2.8 A, T_J = 25°C			0.48		Ω
		Source driver, I_{OUT} = –2.8 A, T_J = 125°C			0.74	0.85	
		Sink driver, I_{OUT} = –2.8 A, T_J = 25°C			0.35		
		Sink driver, I_{OUT} = –2.8 A, T_J = 125°C			0.52	0.7	
V_{TRP}	SENSE trip voltage	R_{SENSE} between SENSE and GND			500		mV
V_f	Body diode forward voltage	Source diode, I_f = –2.8 A				1.4	V
		Sink diode, I_f = 2.8 A				1.4	
t_{pd}	Propagation delay time	INx, Change to source or sink ON			600		ns
		INx, Change to source or sink OFF			100		
t_{COD}	Crossover delay				500		ns
DAGain	Differential amplifier gain	Sense = 0.1 V to 0.4 V			5		V/V
Protection Circuits							
V_{UVLO}	VBB undervoltage lockout	VBB rising			6.5	7.5	V
V_{CPUV}	VCP undervoltage lockout(1)	VBB rising; CPUV recovery			12	13.8	V
I_{OCP}	Overcurrent protection trip level			3			A
t_{DEG}	Overcurrent deglitch time				3.0		µs
t_{OCP}	Overcurrent retry time				1.6		ms
T_{OTW}	Thermal shutdown temperature	Die temperature T_j			160		°C
$T_{OTW\ HYS}$	Thermal shutdown hysteresis	Die temperature T_j			15		°C
T_{OTS}	Thermal shutdown hysteresis	Die temperature T_j			175		°C
$T_{OTS\ HYS}$	Thermal shutdown hysteresis	Die temperature T_j			15		°C

(1) Whenever VCP is less than VM + 10 V, a CPUV event occurs. This fault will be asserted whenever VBB is below 12 V. Note that the H-bridges will remain enabled until VBB = V_{UVLO} even through nFAULT is pulled low.

FUNCTIONAL DESCRIPTION

Power Supervisor

Control input nSLEEP is used to minimize power consumption when the DRV8816 is not in use. This disables much of the internal circuitry, including the internal voltage rails and charge pump. nSLEEP is asserted low. A logic high on this input pin results in normal operation. When switching from low to high, the user should allow a 1-ms delay before applying PWM signals. This time is needed for the charge pump to stabilize.

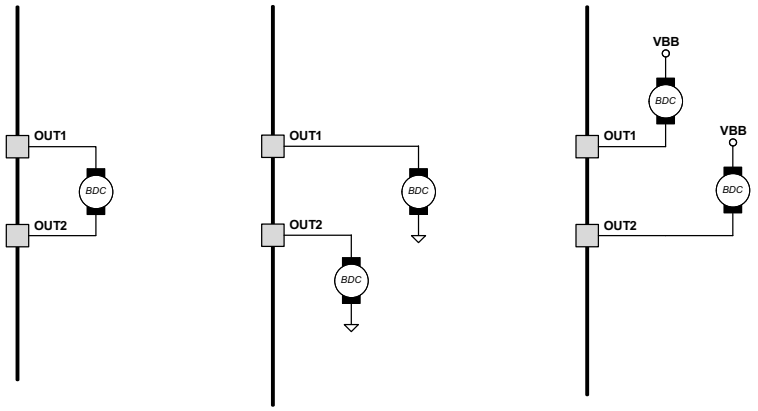
Bridge Control

The DRV8816 is controlled using separate enable and input pins for each ½-H-bridge.

The following table shows the logic for the DRV8816:

ENx	INx	OUTx
0	X	Z
1	0	L
1	1	H

If a single DC motor is connected to the DRV8816, it is connected between the OUT1 and OUT2 pins as shown in the first image below. Two DC motors may also be connected to the DRV8816. In this mode, it is not possible to reverse the direction of the motors; they will turn only in one direction. The connections are shown below:



Motor operation for a single brushed DC motor is controlled as follows:

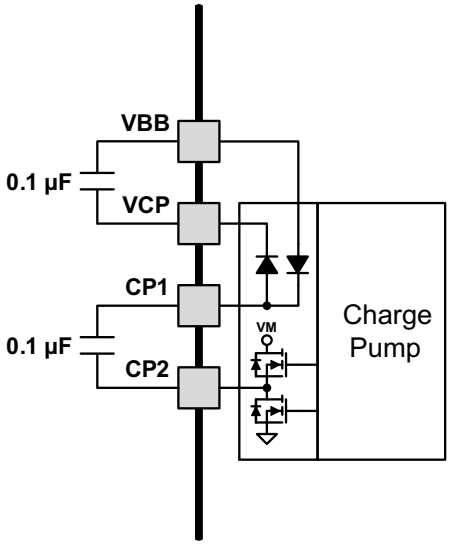
EN1	EN2	IN1	IN2	OUT1	OUT2	Operation
0	X	X	X	Z	See (1)	Off (coast)
X	0	X	X	See (1)	Z	Off (coast)
1	1	0	0	L	L	Brake
1	1	0	1	L	H	Reverse
1	1	1	0	H	L	Forward
1	1	1	1	H	H	Brake

Motor operation for dual brushed DC motors is controlled as follows:

Motor connected to GND	ENx	INx	OUTx	Operation
	0	X	Z	Off (coast)
	1	0	L	Brake
	1	1	H	Forward
Motor connected to VBB	**ENx**	**INx**	**OUTx**	**Operation**
	0	X	Z	Off (coast)
	1	0	L	Forward
	1	1	H	Brake

Charge Pump

The charge pump is used to generate a supply above VBB to drive the source-side DMOS gates. A 0.1-µF ceramic monolithic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1-µF ceramic monolithic capacitor should be connected between VCP and VBB to act as a reservoir to run the high-side DMOS devices. The VCP voltage level is internally monitored and, in the case of a fault condition, the outputs of the device are disabled.

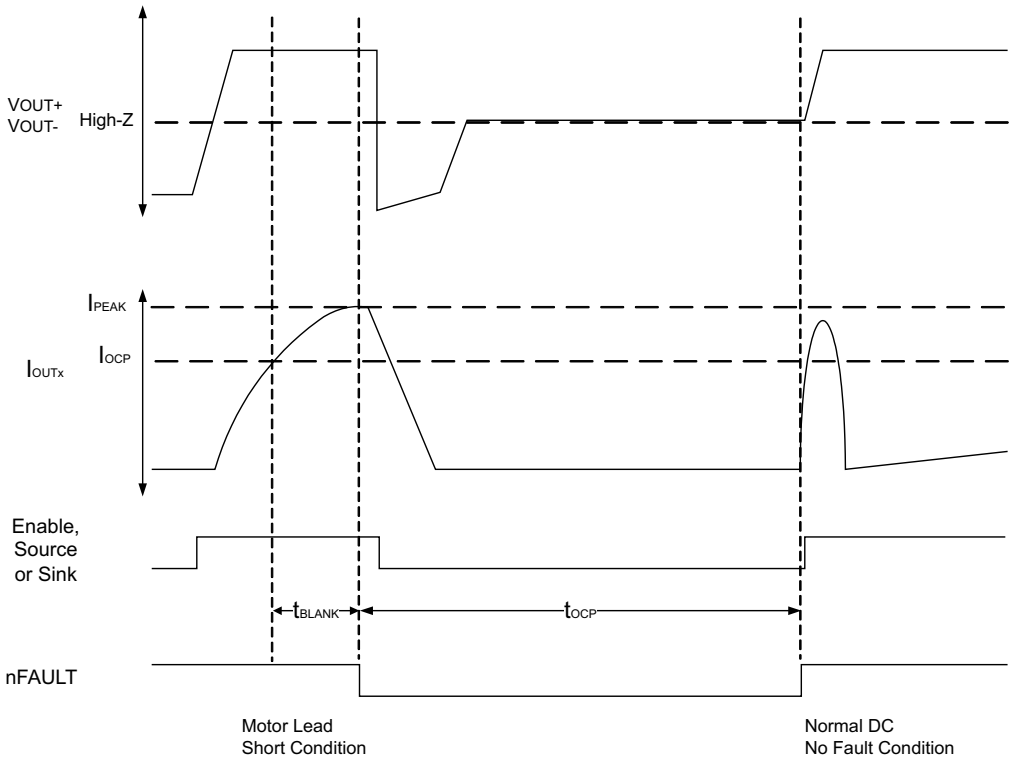


SENSE

A low-value resistor can be placed between the SENSE pin and ground for current-sensing purposes. To minimize ground-trace IR drops in sensing the output current level, the current-sensing resistor should have an independent ground return to the star ground point. This trace should be as short as possible. For low-value sense resistors, the IR drops in the PCB can be significant, and should be taken into account.

To set a manual overcurrent trip threshold, place a resistor between the SENSE pin and GND. When the SENSE pin rises above 500 mV, the H-bridge output is disabled (High-Z). The device will automatically retry with a period of t_{OCP}.

The overcurrent trip threshold can be calculated using I_{trip} = 500 mV/R. The overcurrent trip level selected cannot be greater than I_{OCP}.



VPROPI

The VPROPI output is equal to approximately five times the voltage present on the SENSE pin. VPROPI is meaningful only if there is a resistor connected to the SENSE pin; If SENSE is connected to ground, VPROPI measures 0 V. Also note that during slow decay (brake), VPROPI will measure 0 V. VPROPI can output a maximum of 2.5 V, since at 500 mV on SENSE, the H-bridge is disabled.

Protection Circuits

The DRV8816 is fully protected against VBB undervoltage, charge pump undervoltage, overcurrent, and overtemperature events.

VBB UNDERVOLTAGE LOCKOUT (UVLO)

If at any time the voltage on the VBB pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled and the charge pump will be disabled. Operation will resume when VBB rises above the UVLO threshold. Note that nFAULT does not indicate a UVLO because the CPUV fault is always asserted below VBB = 12 V.

VCP UNDERVOLTAGE LOCKOUT (CPUV)

During a CPUV event, the VCP voltage is measured to be below VCP + 10 V. If at any time the voltage on the VCP pin falls below the undervoltage lockout threshold voltage, the nFAULT pin will be driven low. The nFAULT pin will be released after operation has resumed. Note that this fault does not disable the output FETs and allows the device to continue operating. When VBB is below 12 V, this fault condition is always asserted and nFAULT is pulled low.

OVERCURRENT PROTECTION (OCP)

The current flowing through the high-side and low-side drivers is monitored to ensure that the motor lead is not shorted to supply or ground. If a short is detected, all FETs in the H-bridge will be disabled, nFAULT is driven low, and a t_{OCP} fault timer is started. After this period, t_{OCP}, the device is then allowed to follow the input commands and another turn-on is attempted (nFAULT becomes high again during this attempt). If there is still a fault condition, the cycle repeats. If after t_{OCP} expires it is determined the short condition is not present, normal operation resumes and nFAULT is released.

OVERTEMPERATURE WARNING (OTW)

If the die temperature increases past the thermal warning threshold the nFAULT pin will be driven low. Once the die temperature has fallen below the hysteresis level, the nFAULT pin will be released. If the die temperature continues to increase, the device will enter over temperature shutdown as described below.

OVERTEMPERATURE SHUTDOWN (OTS)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the charge pump will be shut down. Once the die temperature has fallen to a safe level operation will automatically resume.

THERMAL INFORMATION

Thermal Protection

If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level. Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8816 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation can be roughly estimated by:

$$P_{TOT} = R_{D(SON)} \times (I_{OUT(RMS)})^2 \quad (1)$$

where P_{TOT} is the total power dissipation, $R_{D(SON)}$) is the resistance of the HS plus LS FETS, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to approximately 0.7× the full-scale output current setting.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

PCB LAYOUT

Ground

A ground power plane should be located as close to DRV8816 as possible. The copper ground plane directly under the PowerPAD package makes a good location. This pad can then be connected to ground for this purpose.

Layout Considerations

The printed circuit board (PCB) should use a heavy ground plane. For optimum electrical and thermal performance, the DRV8816 must be soldered directly onto the board. On the underside of the DRV8816 is a PowerPAD package, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

The load supply pin, VBB, should be decoupled with an electrolytic capacitor (typically 100 µF) in parallel with a ceramic capacitor placed as close as possible to the device. The ceramic capacitors between VCP and VBB, connected to VREG, and between CP1 and CP2 should be as close to the pins of the device as possible, in order to minimize lead inductance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8816PWP	PREVIEW	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8816	
DRV8816PWPR	PREVIEW	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8816	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

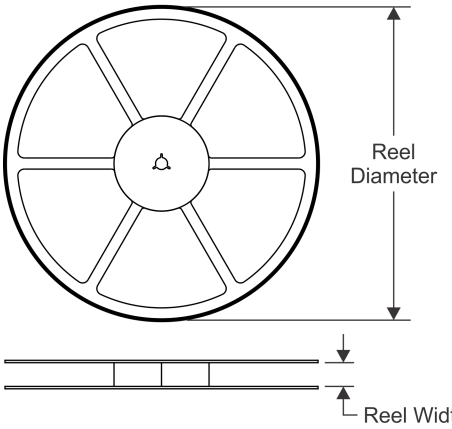
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

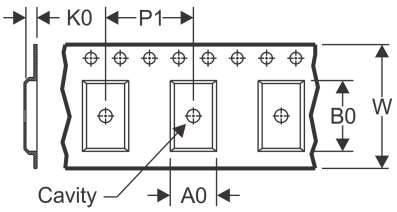
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

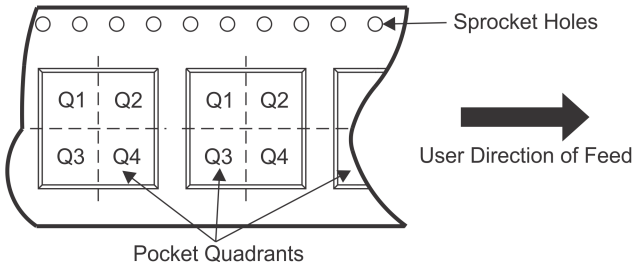


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

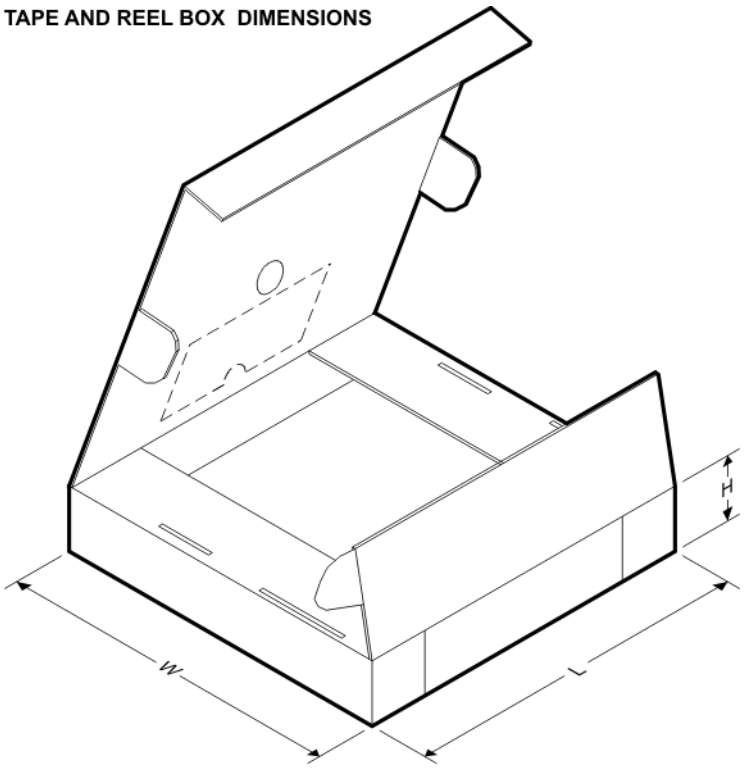
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8816PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

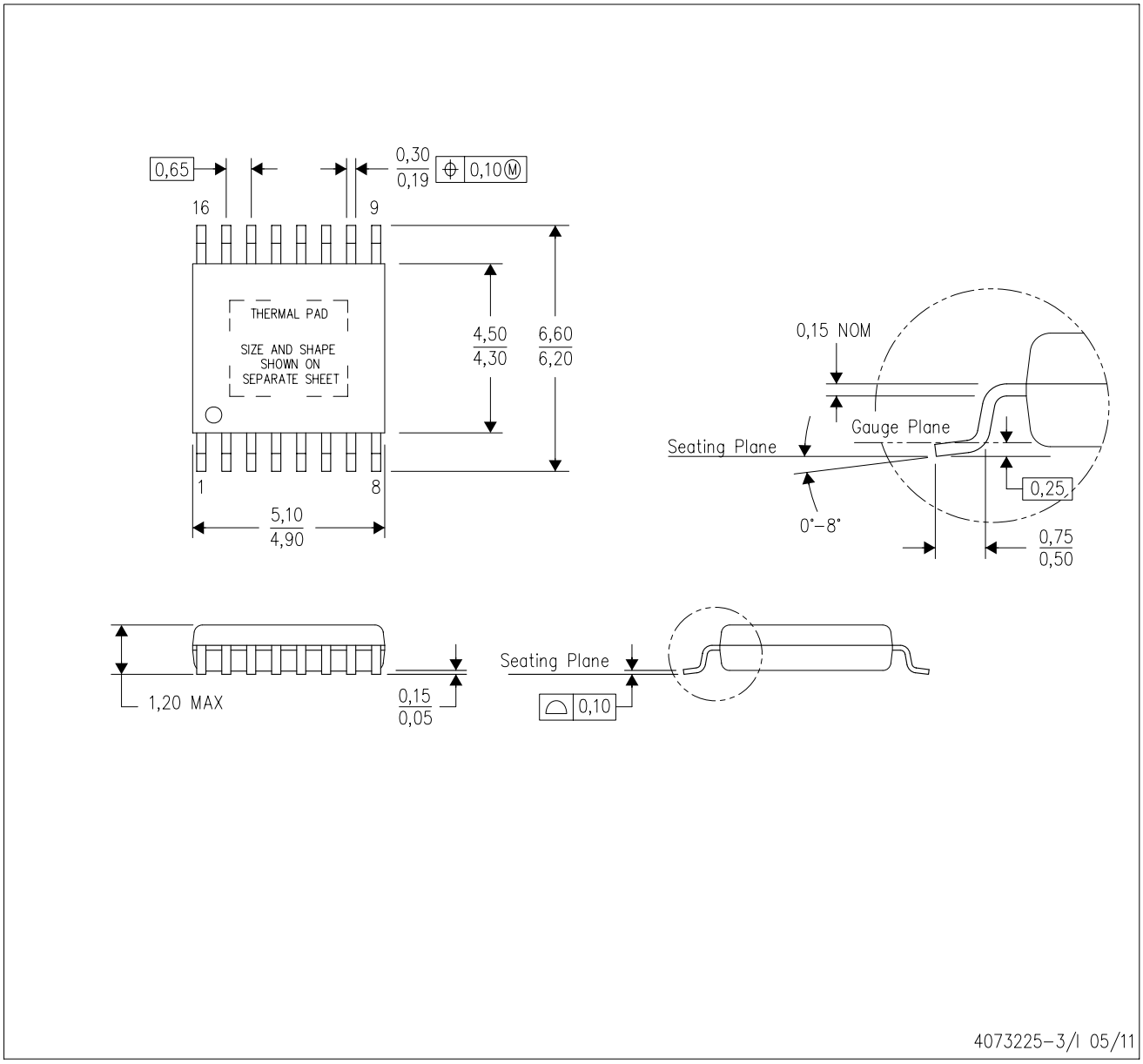
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8816PWPR	HTSSOP	PWP	16	2000	367.0	367.0	35.0

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

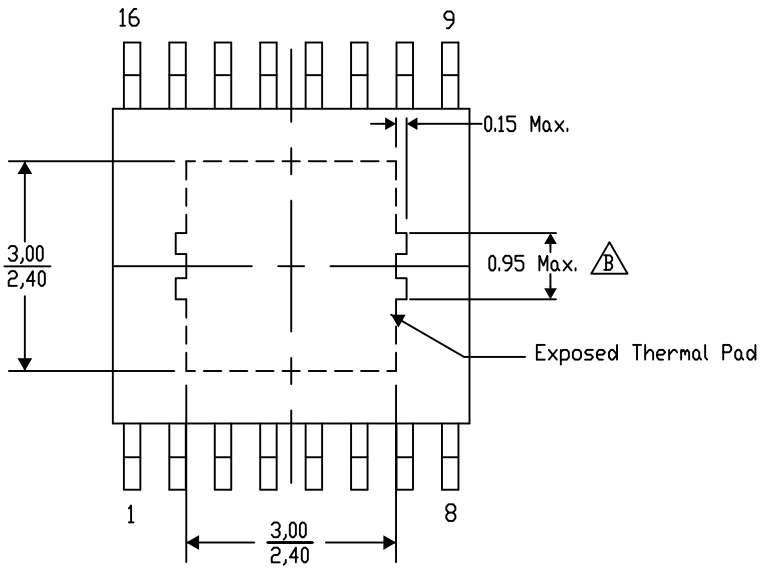
PWP (R–PDSO–G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

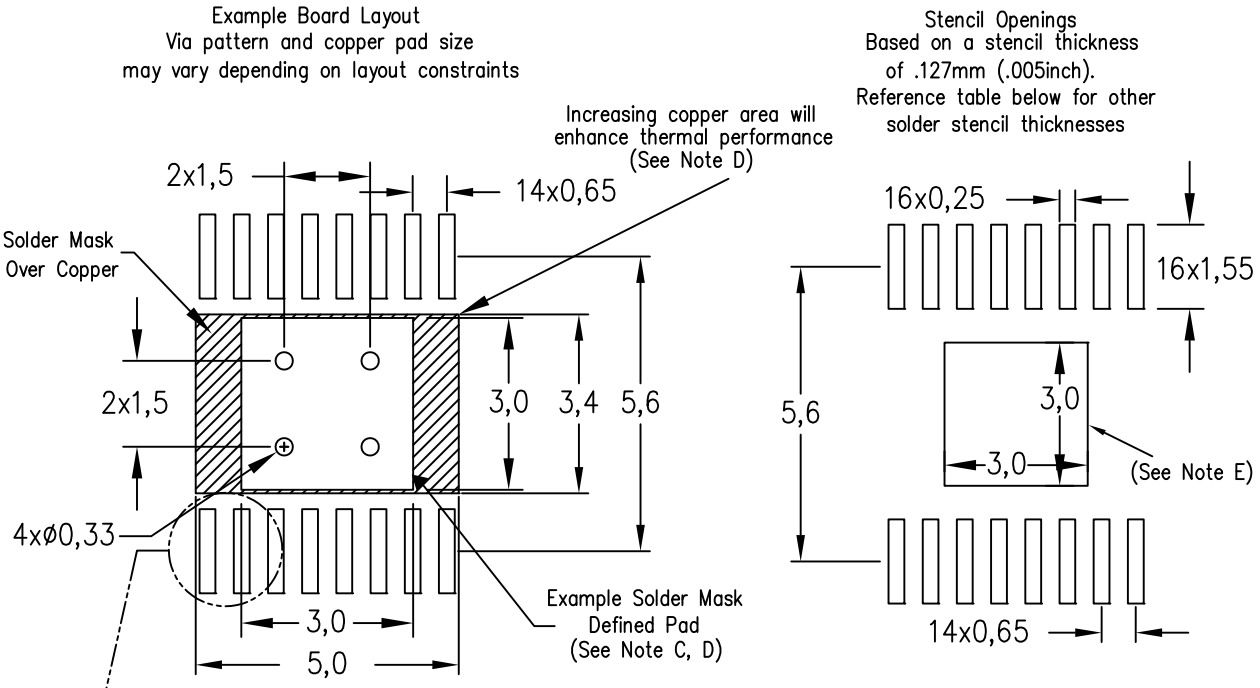
4206332–8/AG 08/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G16) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.2	3.2
0.127mm	3.0	3.0
0.152mm	2.8	2.8
0.178mm	2.6	2.6

4207609–5/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265